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01/09/03

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Application of:

BENOUDIZ, Eyal

Serial No.: 10/045,055

Filed: January 15, 2002

For: System and Method for Visual Debugging  
of Constraint Systems

Examiner:

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Group Art Unit: 2133

Attorney  
Docket: 24773  
(Previously V02/16)

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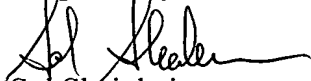
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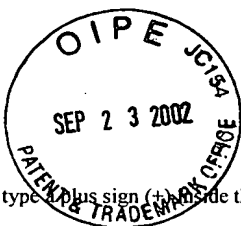
Enclosed is a PTO Form SB/08A which lists citations which may be material to the patentability and examination of the above identified application. Also enclosed are copies of the references cited. These are submitted in compliance with the duty of disclosure defined in 37 CFR 1.56. The Examiner is requested to make these citations of official record in this application.

This Information Disclosure Statement under 37 CFR 1.56 is not to be construed as a representation that a search has been made, that additional matter which is material to the examination of this application does not exist, or that any or more of these citations constitutes prior art.

Respectfully submitted,

  
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Date: September 17, 2002



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PTO/SB/08A (10-96)

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				Application Number	10/045,055
				Filing Date	January 15, 2002
				First Named Inventor	Benoudiz
				Group Art Unit	2133
				Examiner Name	
Sheet	1	of	1	Attorney Docket Number	24773 Previously V02/16

U.S. PATENT DOCUMENTS						
Examiners Initials	Cite No. <sup>1</sup>	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, columns, lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code <sup>2</sup> (if known)			
	AA	4,937,765		Shupe et al	06-26-1990	
	AB	5,202,889		Aharon et al	04-13-1993	
	AC	5,633,812		Allen et al	05-27-1997	
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	AE	6,044,214		Kimura et al	03-28-2000	
	AF	6,059,451		Scott et al	05-09-2000	

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
	AG	Benjamin et al, A Study in Coverage-Driven Test Generation, DAC, 1999, pp. 970 – 975	
	AH	Debany Jr. et al, Design Verification Using Logic Tests, IEEE, 1992, pp. 17 – 24	
	AI	Moundanos, et al., Abstraction Techniques for Validation Coverage Analysis and Test Generation, IEEE Transactions on Computers, Vol. 47, No. 1, January 1998, pp. 2 – 14	
	AJ	Piowowski, Coverage Measurement Experience During Function Test, IEEE Proc. 15 <sup>th</sup> Int. Conf. Software Engineering, 1993, pp 287 – 301	
	AK	Greggain et al, Fault Grading, A Measure of Logic Simulation Integrity, Proc. 2 <sup>nd</sup> Annual IEEE ASIC Seminar and Exhibit, 1989, pp 9-2.1 – 9-2.4	
	AL	Sneed, State Coverage of Embedded Realtime Programs, Proc. 2 <sup>nd</sup> Workshop on Software Testing, Verification & Analysis, 1988, pp 245	

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